

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 7,103,041 B1  
APPLICATION NO. : 09/610116  
DATED : September 5, 2006  
INVENTOR(S) : Speiser et al.

Page 1 of 19

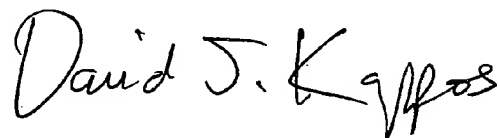
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Under Columns 21-56, delete handwritten numbers “41”, “42”, “43”, “44”, “45”, “46”, “47”, “48”, “49”, “50”, “51”, “52”, “53”, “54”, “55”, “56”, “57”, “58”.

In Column 26, below Figure, Line 2, delete “disab” and insert -- disabled) --, therefor.

Signed and Sealed this

Twenty-sixth Day of January, 2010

A handwritten signature in black ink that reads "David J. Kappos". The signature is written in a cursive, flowing style with a large initial 'D' and a stylized 'K'.

David J. Kappos  
*Director of the United States Patent and Trademark Office*

**APPENDIX**

BFS Backplane Optimization Worksheet

Notes:

1) Colors are used to represent the use/reuse of serial communication channels.



used in next config (off limits for this config)  
2nd use of receiver/transmitter  
3rd use of receiver/transmitter

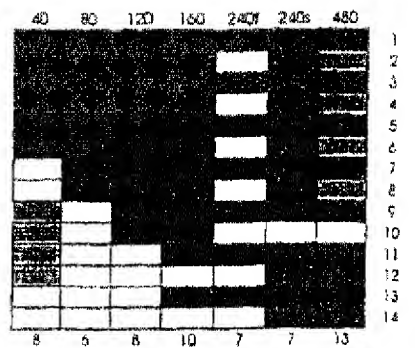
2) Channel assignments are optimized for multiple variables.

- Minimization of I/O. Quad GE transceivers provide 1:2 fanout buffers and 2:1 multiplexers. 1:3 fanout or 3:1 fanin requires additional external devices.

- Partitioning of PCB routing complexity. The ASIC to quad GE buses are ideally straight and interleaved (striper with unstriper and aggregator with separator) to simplify the routing of these clocked buses. The serial connections from quad GE transceivers to card edge connector on fabric and blocks require significant untangling (with minimal use of vias) to group signals by common destination on the edge connector. This is required to reduce the complexity of the backplane routing and corresponding layer count.

- Minimization of symmetry between ASIC's. This symmetry allows interleaving of buses and reduces the need for external mux's and fanout buffers. It may also reduce the complexity of ASICs by reducing the number of unique mux/demux structures. Consequently, the striper map is a subset of the unstriper map, and both aggregator maps and the separator 5:8 map are derived from the separator 1:4 map.

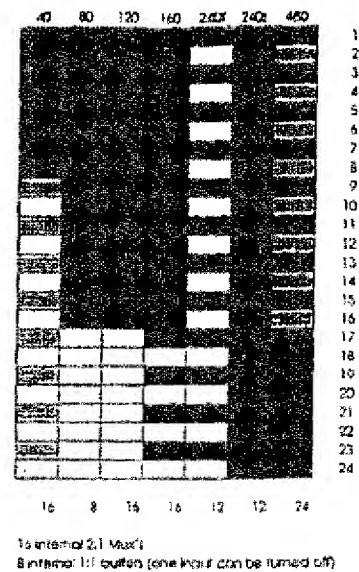
Striper		8	6	8	10	7	7	13
# active fx		10		10		7		13
# fabrics		1	2	3	4	6	6	12
configuration		40	80	120	160	240f	240s	480
S_1A1		1	1	1	1	1	1	1
S_1A2		2	2	2	2			
S_1A3		11						
S_1A4		9						
F1_1A1		3	3	3	3	3	3	3
F1_1A2		4	4	4	4			
F1_1A3		12						
F1_1A4		10						
F2_1A1		5	5	5	5	5	5	5
F2_1A2		6	6	6				
F3_1A1		7	7	7	7	7		
F3_1A2		8	8					
F4_1A1		9	9	9	9			
F4_1A2		10						
F5_1A1		11	11	11	11			
F6_1A1		13	13	13				
F7_1A1		2						
F8_1A1		4						
F9_1A1		6						
F10_1A1		8						
F11_1A1		12						
F12_1A1		14						
Total		22						



8 internal 1:2 fanout buffers  
6 internal 1:1 fanout buffers (one output can be disabled)

		Aggregates 1-4											
Aggregate 1		16	8	16	16	12	12	24					
Aggregate 2		16	16	16	16	12	12	24					
Aggregate 3		1	2	3	4	6	6	12					
Aggregate 4		40	80	120	160	240	240	480					
FI_1A1	1A	1	1	1	1	1	1	1	1	1	1	1	1
FI_1A2	1A	2	2	2	2								
FI_1A3	1A	17											
FI_1A4	1A	6											
FI_1B1	1B	3	3	3	3	3	3	3	3	3	3	3	3
FI_1B2	1B	4	4	4	4								
FI_1B3	1B	19											
FI_1B4	1B	1											
FI_1C1	1C	5	5	5	5	5	5	5	5	5	5	5	5
FI_1C2	1C	6	6	6	6								
FI_1C3	1C	21											
FI_1C4	1C	13											
FI_1D1	1D	7	7	7	7	7	7	7	7	7	7	7	7
FI_1D2	1D	8	8	8	8								
FI_1D3	1D	23											
FI_1D4	1D	15											
FI_9A1	9A	9	9	9	9	9							
FI_9A2	9A	10	10										
FI_9B1	9B	11	11	11	11	11							
FI_9B2	9B	12	12										
FI_9C1	9C	13	13	13	13	13							
FI_9C2	9C	14	14										
FI_9D1	9D	15	15	15	15	15							
FI_9D2	9D	16	16										
FI_17A1	17A	17	17	17									
FI_17B1	17B	19	19	19									
FI_17C1	17C	21	21	21									
FI_17D1	17D	23	23	23									
FI_25A1	25A	2											
FI_25B1	25B	4											
FI_25C1	25C	6											
FI_25D1	25D	8											
FI_33A1	33A	10											
FI_33B1	33B	12											
FI_33C1	33C	14											
FI_33D1	33D	16											
FI_41A1	41A	18											
FI_41B1	41B	20											
FI_41C1	41C	22											
FI_41D1	41D	24											

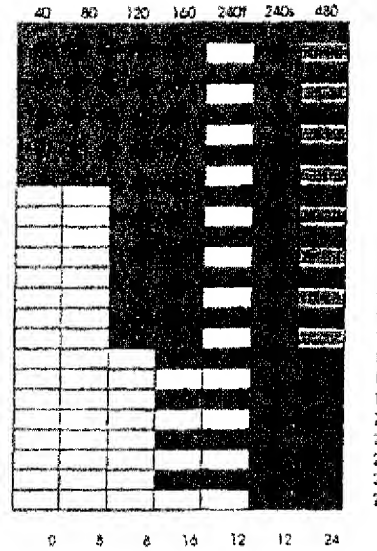
increments by 8      40 total



16 internal 2:1 Max's  
8 internal 1:1 buffer (one hour can be turned off)

		Approx. 5-8									
Active rx		0	8	16	24	32	40	48	56		
Status		0	8	16	24	32	40	48	56		
Configuration		40	80	120	160	240	280	320	400		
FI_5A1	5A	1	1	1	1	1	1	1	1	1	1
FI_5A2	5A	2	2	2	2	2	2	2	2	2	2
FI_5B1	5B	3	3	3	3	3	3	3	3	3	3
FI_5B2	5B	4	4	4	4	4	4	4	4	4	4
FI_5C1	5C	5	5	5	5	5	5	5	5	5	5
FI_5C2	5C	6	6	6	6	6	6	6	6	6	6
FI_5D1	5D	7	7	7	7	7	7	7	7	7	7
FI_5D2	5D	8	8	8	8	8	8	8	8	8	8
FI_13A1	13A	9	9	9	9	9	9	9	9	9	9
FI_13A2	13A	10	10	10	10	10	10	10	10	10	10
FI_13B1	13B	11	11	11	11	11	11	11	11	11	11
FI_13B2	13B	12	12	12	12	12	12	12	12	12	12
FI_13C1	13C	13	13	13	13	13	13	13	13	13	13
FI_13C2	13C	14	14	14	14	14	14	14	14	14	14
FI_13D1	13D	15	15	15	15	15	15	15	15	15	15
FI_13D2	13D	16	16	16	16	16	16	16	16	16	16
FI_21A1	21A	17	17	17	17	17	17	17	17	17	17
FI_21B1	21B	18	18	18	18	18	18	18	18	18	18
FI_21C1	21C	19	19	19	19	19	19	19	19	19	19
FI_21D1	21D	20	20	20	20	20	20	20	20	20	20
FI_29A1	29A	21	21	21	21	21	21	21	21	21	21
FI_29B1	29B	22	22	22	22	22	22	22	22	22	22
FI_29C1	29C	23	23	23	23	23	23	23	23	23	23
FI_29D1	29D	24	24	24	24	24	24	24	24	24	24
FI_37A1	37A	25	25	25	25	25	25	25	25	25	25
FI_37B1	37B	26	26	26	26	26	26	26	26	26	26
FI_37C1	37C	27	27	27	27	27	27	27	27	27	27
FI_37D1	37D	28	28	28	28	28	28	28	28	28	28
FI_45A1	45A	29	29	29	29	29	29	29	29	29	29
FI_45B1	45B	30	30	30	30	30	30	30	30	30	30
FI_45C1	45C	31	31	31	31	31	31	31	31	31	31
FI_45D1	45D	32	32	32	32	32	32	32	32	32	32

32 total

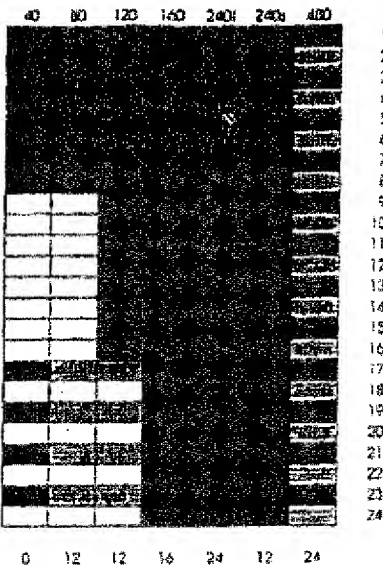


8 internal 2:1 Mux's  
16 internal 1:1 buffers (one input can be turned off)

Separator 1-4									
Port	1	2	3	4	5	6	7	8	9
1	20	12	16	16	24	10	24		
2	20		24		24		24		
3		20		24		24			
4			20		24				
5				20		24			
6					20		24		
7						20		24	
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Subprocessor 5-B									
# active n		0	12	12	16	24	12	24	
# buffers		12	20	24	24	24	24	24	
Configuration		40	80	120	160	240	240	480	
FI_5A1	5A	1	1	1	1	1	1	1	1
FI_5A2	5A	2	2	2	2				2
FI_5A3	5A	17	17						17
FI_5B1	5B	3	3	3	3	3	3		3
FI_5B2	5B	4	4	4	4				4
FI_5B3	5B	19	19						19
FI_5C1	5C	5	5	5	5	5	5		5
FI_5C2	5C	6	6	6	6				6
FI_5C3	5C	21	21						21
FI_5D1	5D	7	7	7	7	7	7		7
FI_5D2	5D	8	8	8	8				8
FI_5D3	5D	23	23						23
FI_13A1	13A	9	9	9	9				9
FI_13A2	13A	10	10						10
FI_13B1	13B	11	11	11	11				11
FI_13B2	13B	12	12						12
FI_13C1	13C	13	13	13	13				13
FI_13C2	13C	14	14						14
FI_13D1	13D	15	15	15	15				15
FI_13D2	13D	16	16						16
FI_21A1	21A	17	17	17					17
FI_21A2	21A	18							18
FI_21B1	21B	19	19	19					19
FI_21B2	21B	20							20
FI_21C1	21C	21	21	21					21
FI_21C2	21C	22							22
FI_21D1	21D	23	23	23					23
FI_21D2	21D	24							24
FI_29A1	29A		2						2
FI_29B1	29B		4						4
FI_29C1	29C		6						6
FI_29D1	29D		8						8
FI_37A1	37A		10						10
FI_37B1	37B		12						12
FI_37C1	37C		14						14
FI_37D1	37D		16						16
FI_45A1	45A		18						18
FI_45B1	45B		20						20
FI_45C1	45C		22						22
FI_45D1	45D		24						24

40 total

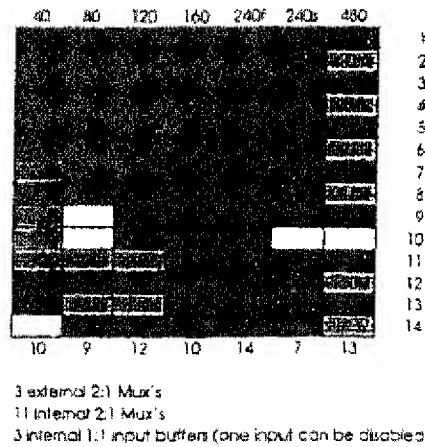


16 internal 1:2 fanout buffers  
12 internal 1:1 buffers (one output can be turned off)



Unstriper							
# active rx	10	9	12	10	14	7	13
# fabrics	1	2	3	4	6	6	12
Configuration	40	80	120	160	240f	240s	480
S_1A1	1	1	1	1	1	1	1
S_1A2	2	2	2	2	2		
S_1A3	11	11	11				
S_1A4	9						
S_1A5	7						
F1_1A1	3	3	3	3	3	3	3
F1_1A2	4	4	4	4	4		
F1_1A3	12	12	12				
F1_1A4	10						
F1_1A5	8						
F2_1A1	5	5	5	5	5	5	
F2_1A2	6	6	6	6			
F2_1A3	13	13					
F3_1A1	7	7	7	7	7		
F3_1A2	8	8	8				
F3_1A3	14						
F4_1A1	9	9	9	9			
F4_1A2	10	10					
F5_1A1	11	11	11				
F5_1A2	12						
F6_1A1	13	13	13				
F6_1A2	14						
F7_1A1					2		
F8_1A1					4		
F9_1A1					6		
F10_1A1					8		
F11_1A1					12		
F12_1A1					14		

Total 28




gfs ASIC Blockplane Connection Map

Revision	Date	Comments
1	11/31/99	First release, checked by Speiser
2	11/6/99	Changed AGG assignments for channels 7 and 9; corrects the sliper and unslipeir only
		Changed AGG, 120G assignments for channels 17-24 to make Separator 1-4 and Separator 5-8 symmetric (Separator 5-8 is now a subset of Separator 1-4)
3	11/30/99	Corrected by Speiser and Banerjee
		Added control port assignments

Fabric to Blade egress bus format: <fabric> <blades> <channels> <slanes> <ports>
Fabric slot Blade slot Channel Lane Port
F1-F123 1-48 A-D 1-5 P-N

Noting convention:

Notes:

- 1) Map shown for a single instance of each ASIC, e.g. sliper channel A for blade number 1. From an ASIC point of view, cell that is significant in this sliper table is the fabric number and the lane number. The topology is the same for each subsequent channel (B-D) blade slot (7-48).
- 2) Polarity is required to distinguish the two physical wires forming a differential pair. For each table entry (e.g., each logical signal) there are two physical connections. For example, logical signal F2\_1A3 is really comprised of F2\_1A3P and F2\_1A3N, which connect fabric 2 to blade 1, unslipeir 1, lane 3. Polarity is not shown in the connection maps to make them easier to read.
- 3) How to use this map: For a given configuration (e.g. with one fabric installed, read down AGG column). Read down the column to determine the source for data present on a sliper output bus. Each row represents a single sliper output bus.
- 4)  = not used in this Configuration
- 5) To aid in PCB routing and reduce design complexity, there are only two unique connection assignments, the unslipeir and the Separator 1-4 maps. The sliper map is a subset of the unslipeir map. The separator 5-8 map, the aggregator 1-4 map, and the aggregator 5-8 map are all subsets of the separator 1-4 map.
- 6) Up to four control ports are supported (see maps for aggregator 9 and separator 9). If not all four control ports are needed, some control port channels can be deleted. For example, if only two 25Gbps control ports are needed, control port channels C and D can be ignored.

Configuration							Slipper Output bus
40	60	120	160	240f	240s	480	
S_1A1	S_1A1	S_1A1	S_1A1	S_1A1	S_1A1	S_1A1	1
S_1A2	S_1A2	S_1A2	S_1A2			F7_1A1	2
F1_1A1	F1_1A1	F1_1A1	F1_1A1	F1_1A1	F1_1A1	F1_1A1	3
F1_1A2	F1_1A2	F1_1A2	F1_1A2			F8_1A1	4
	F2_1A1	F2_1A1	F2_1A1	F2_1A1	F2_1A1	F2_1A1	5
	F2_1A2	F2_1A2	F2_1A2			F9_1A1	6
		F3_1A1	F3_1A1	F3_1A1	F3_1A1	F3_1A1	7
		F3_1A2	F3_1A2			F10_1A1	8
			F4_1A1	F4_1A1	F4_1A1	F4_1A1	9
S_1A4			F4_1A2				10
F1_1A4				F5_1A1	F5_1A1	F5_1A1	11
S_1A3						F11_1A1	12
F1_1A3				F6_1A1	F6_1A1	F6_1A1	13
						F12_1A1	14

Aggregator 1-4									
Configuration									
40	80	120	160	240f	240s	480	Aggregator Input bus		
F1_1A1	F1_1A1	F1_1A1	F1_1A1	F1_1A1	F1_1A1	F1_1A1	1		
F1_1A2	F1_1A2	F1_1A2	F1_1A2			F1_25A1	2		
F1_1B1	F1_1B1	F1_1B1	F1_1B1	F1_1B1	F1_1B1	F1_1B1	3		
F1_1B2	F1_1B2	F1_1B2	F1_1B2			F1_25B1	4		
F1_1C1	F1_1C1	F1_1C1	F1_1C1	F1_1C1	F1_1C1	F1_1C1	5		
F1_1C2	F1_1C2	F1_1C2	F1_1C2			F1_25C1	6		
F1_1D1	F1_1D1	F1_1D1	F1_1D1	F1_1D1	F1_1D1	F1_1D1	7		
F1_1D2	F1_1D2	F1_1D2	F1_1D2			F1_25D1	8		
F1_1A4		F1_9A1	F1_9A1	F1_9A1	F1_9A1	F1_9A1	9		
		F1_9A2	F1_9A2			F1_33A1	10		
F1_1B4		F1_9B1	F1_9B1	F1_9B1	F1_9B1	F1_9B1	11		
		F1_9B2	F1_9B2			F1_33B1	12		
F1_1C4		F1_9C1	F1_9C1	F1_9C1	F1_9C1	F1_9C1	13		
		F1_9C2	F1_9C2			F1_33C1	14		
F1_1D4		F1_9D1	F1_9D1	F1_9D1	F1_9D1	F1_9D1	15		
		F1_9D2	F1_9D2			F1_33D1	16		
F1_1A3				F1_17A1	F1_17A1	F1_17A1	17		
						F1_41A1	18		
F1_1B3				F1_17B1	F1_17B1	F1_17B1	19		
						F1_41B1	20		
F1_1C3				F1_17C1	F1_17C1	F1_17C1	21		
						F1_41C1	22		
F1_1D3				F1_17D1	F1_17D1	F1_17D1	23		
						F1_41D1	24		

Aggregator 5-A								Aggregator Input bus
Configuration								
40	80	120	160	240f	240s	480		
	F1_5A1	F1_5A1	F1_5A1	F1_5A1	F1_5A1	F1_5A1	1	
	F1_5A2	F1_5A2	F1_5A2			F1_29A1	2	
	F1_5B1	F1_5B1	F1_5B1	F1_5B1	F1_5B1	F1_5B1	3	
	F1_5B2	F1_5B2	F1_5B2			F1_29B1	4	
	F1_5C1	F1_5C1	F1_5C1	F1_5C1	F1_5C1	F1_5C1	5	
	F1_5C2	F1_5C2	F1_5C2			F1_29C1	6	
	F1_5D1	F1_5D1	F1_5D1	F1_5D1	F1_5D1	F1_5D1	7	
	F1_5D2	F1_5D2	F1_5D2			F1_29D1	8	
			F1_13A1	F1_13A1	F1_13A1	F1_13A1	9	
			F1_13A2			F1_37A1	10	
			F1_13B1	F1_13B1	F1_13B1	F1_13B1	11	
			F1_13B2			F1_37B1	12	
			F1_13C1	F1_13C1	F1_13C1	F1_13C1	13	
			F1_13C2			F1_37C1	14	
			F1_13D1	F1_13D1	F1_13D1	F1_13D1	15	
			F1_13D2			F1_37D1	16	
				F1_21A1	F1_21A1	F1_21A1	17	
				F1_21B1	F1_21B1	F1_45A1	18	
						F1_21B1	19	
				F1_21C1	F1_21C1	F1_45B1	20	
						F1_21C1	21	
						F1_45C1	22	
				F1_21D1	F1_21D1	F1_21D1	23	
						F1_45D1	24	

Configuration								Aggregator Input bus
40	80	120	160	240i	240s	480		
F1_CP_A1	F1_CP_A1	F1_CP_A1	F1_CP_A1	F1_CP_A1	F1_CP_A1	F1_CP_A1	1	
F1_CP_A2	F1_CP_A2	F1_CP_A2	F1_CP_A2				2	
F1_CP_B1	F1_CP_B1	F1_CP_B1	F1_CP_B1	F1_CP_B1	F1_CP_B1	F1_CP_B1	3	
F1_CP_D2	F1_CP_D2	F1_CP_D2	F1_CP_B2				4	
F1_CP_C1	F1_CP_C1	F1_CP_C1	F1_CP_C1	F1_CP_C1	F1_CP_C1	F1_CP_C1	5	
F1_CP_C2	F1_CP_C2	F1_CP_C2	F1_CP_C2				6	
F1_CP_D1	F1_CP_D1	F1_CP_D1	F1_CP_D1	F1_CP_D1	F1_CP_D1	F1_CP_D1	7	
F1_CP_D2	F1_CP_D2	F1_CP_D2	F1_CP_D2				8	
F1_CP_A4							9	
F1_CP_B4							10	
F1_CP_C4							11	
F1_CP_D4							12	
F1_CP_A3							13	
F1_CP_D3							14	
F1_CP_C3							15	
F1_CP_D3							16	
F1_CP_C3							17	
F1_CP_D3							18	
F1_CP_C3							19	
F1_CP_D3							20	
F1_CP_C3							21	
F1_CP_D3							22	
F1_CP_C3							23	
F1_CP_D3							24	

Separator 1-4										Separator
Configuration										bus
40	80	120	160	240r	240s	480				bus
FI_1A1	FI_1A1	FI_1A1	FI_1A1	FI_1A1	FI_1A1	FI_1A1				1
FI_1A2	FI_1A2	FI_1A2	FI_1A2	FI_1A2		FI_2B41				2
FI_1B1	FI_1B1	FI_1B1	FI_1B1	FI_1B1	FI_1B1	FI_1B1				3
FI_1B2	FI_1B2	FI_1B2	FI_1B2	FI_1B2		FI_2B81				4
FI_1C1	FI_1C1	FI_1C1	FI_1C1	FI_1C1	FI_1C1	FI_1C1				5
FI_1C2	FI_1C2	FI_1C2	FI_1C2	FI_1C2		FI_2SC1				6
FI_1D1	FI_1D1	FI_1D1	FI_1D1	FI_1D1	FI_1D1	FI_1D1				7
FI_1D2	FI_1D2	FI_1D2	FI_1D2	FI_1D2		FI_2SD1				8
FI_1A4		FI_9A1	FI_9A1	FI_9A1	FI_9A1	FI_9A1				9
FI_1A5		FI_9A2	FI_9A2	FI_9A2		FI_3SA1				10
FI_1B4		FI_9B1	FI_9B1	FI_9B1	FI_9B1	FI_9B1				11
FI_1B5		FI_9B2	FI_9B2	FI_9B2		FI_3SB1				12
FI_1C4		FI_9C1	FI_9C1	FI_9C1	FI_9C1	FI_9C1				13
FI_1C5		FI_9C2	FI_9C2	FI_9C2		FI_3SC1				14
FI_1D4		FI_9D1	FI_9D1	FI_9D1	FI_9D1	FI_9D1				15
FI_1D5		FI_9D2	FI_9D2	FI_9D2		FI_3SD1				16
FI_1A3	FI_1A3	FI_1A3		FI_17A1	FI_17A1	FI_17A1				17
FI_1B3	FI_1B3	FI_1B3		FI_17B2		FI_41A1				16
				FI_17B1	FI_17B1	FI_41B1				19
FI_1C3	FI_1C3	FI_1C3		FI_17C1	FI_17C1	FI_17C1				21
FI_1D3	FI_1D3	FI_1D3		FI_17C2		FI_41C1				22
				FI_17D1	FI_17D1	FI_17D1				23
		FI_9D3		FI_17D2		FI_41D1				24

Separator 5-b

Configuration							Separator output bus
40	80	120	160	240 <sup>a</sup>	240 <sup>b</sup>	480	1
	F1_5A1	F1_5A1	F1_5A1	F1_5A1	F1_5A1	F1_5A1	2
	F1_5A2	F1_5A2	F1_5A2	F1_5A2		F1_29A1	3
	F1_5B1	F1_5B1	F1_5B1	F1_5B1	F1_5B1	F1_5B1	4
	F1_5B2	F1_5B2	F1_5B2	F1_5B2		F1_29B1	5
	F1_5C1	F1_5C1	F1_5C1	F1_5C1	F1_5C1	F1_5C1	6
	F1_5C2	F1_5C2	F1_5C2	F1_5C2		F1_29C1	7
	F1_5D1	F1_5D1	F1_5D1	F1_5D1	F1_5D1	F1_5D1	8
	F1_5D2	F1_5D2	F1_5D2	F1_5D2		F1_29D1	9
			F1_13A1	F1_13A1	F1_13A1	F1_13A1	10
			F1_13A2	F1_13A2		F1_37A1	11
			F1_13B1	F1_13B1	F1_13B1	F1_13B1	12
			F1_13B2	F1_13B2		F1_37B1	13
			F1_13C1	F1_13C1	F1_13C1	F1_13C1	14
			F1_13C2	F1_13C2		F1_37C1	15
			F1_13D1	F1_13D1	F1_13D1	F1_13D1	16
			F1_13D2	F1_13D2		F1_37D1	17
	F1_5A3	F1_5A3		F1_21A1	F1_21A1	F1_21A1	18
	F1_5B3	F1_5B3		F1_21A2		F1_45A1	19
				F1_21B1	F1_21B1	F1_21B1	20
	F1_5C3	F1_5C3		F1_21B2		F1_45B1	21
				F1_21C1	F1_21C1	F1_21C1	22
				F1_21C2		F1_45C1	23
	F1_5D3	F1_5D3		F1_21D1	F1_21D1	F1_21D1	24
				F1_21D2		F1_45D1	



Separator 6							Separator output bus
Configuration							
40	80	120	160	240t	240s	480	
F1_CP_A1	F1_CP_A1	F1_CP_A1	F1_CP_A1	F1_CP_A1	F1_CP_A1	F1_CP_A1	
F1_CP_A2	F1_CP_A2	F1_CP_A2	F1_CP_A2	F1_CP_A2			
F1_CP_B1	F1_CP_B1	F1_CP_B1	F1_CP_D1	F1_CP_B1	F1_CP_B1	F1_CP_B1	
F1_CP_B2	F1_CP_B2	F1_CP_B2	F1_CP_U2	F1_CP_B2			
F1_CP_C1	F1_CP_C1	F1_CP_C1	F1_CP_C1	F1_CP_C1	F1_CP_C1	F1_CP_C1	
F1_CP_C2	F1_CP_C2	F1_CP_C2	F1_CP_C2	F1_CP_C2			
F1_CP_D1	F1_CP_D1	F1_CP_D1	F1_CP_D1	F1_CP_D1	F1_CP_D1	F1_CP_D1	
F1_CP_D2	F1_CP_D2	F1_CP_D2	F1_CP_D2	F1_CP_D2			
F1_CP_A4							
F1_CP_A5							
F1_CP_B4							
F1_CP_B5							
F1_CP_C4							
F1_CP_C5							
F1_CP_D4							
F1_CP_D5							
F1_CP_A3	F1_CP_A3	F1_CP_A3					
F1_CP_B3	F1_CP_B3	F1_CP_B3					
F1_CP_C3	F1_CP_C3	F1_CP_C3					
F1_CP_D3	F1_CP_D3	F1_CP_D3					

Unzipper Configuration								Unzipper Input bus
40	80	120	160	240	240s	480		
S_1A1	S_1A1	S_1A1	S_1A1	S_1A1	S_1A1	S_1A1	1	
S_1A2	S_1A2	S_1A2	S_1A2	S_1A2		F7_1A1	2	
F1_1A1	F1_1A1	F1_1A1	F1_1A1	F1_1A1	F1_1A1	F1_1A1	3	
F1_1A2	F1_1A2	F1_1A2	F1_1A2	F1_1A2		F0_1A1	4	
	F2_1A1	F2_1A1	F2_1A1	F2_1A1	F2_1A1	F2_1A1	5	
	F2_1A2	F2_1A2	F2_1A2			F9_1A1	6	
S_1A5		F3_1A1	F3_1A1	F3_1A1	F3_1A1	F3_1A1	7	
F1_1A5		F3_1A2	F3_1A2	F3_1A2		F10_1A1	8	
S_1A6			F4_1A1	F4_1A1	F4_1A1	F4_1A1	9	
F1_1A4			F4_1A2				10	
S_1A3	S_1A1	S_1A3		F5_1A1	F5_1A1	F0_1A1	11	
F1_1A3	F1_1A3	F1_1A3		F5_1A2		F11_1A1	12	
	F2_1A3	F2_1A3		F6_1A1	F6_1A1	F0_1A1	13	
		F3_1A3		F6_1A2		F12_1A1	14	

**စာအုပ်အမျိုးအမည်**

കുടുംബശ്രീയുടെ സഹായത്തോടെ പല കുടുംബങ്ങളും സാമ്പത്തികമായി സ്വതന്ത്രമായിത്തീർന്നു.

[illegible]

- c- physical
- c- does not include space
- c- number of 750MHz data bits from server to edge router per OC-48 (1% per port card)

Chouhanchi  
shipped to Tokyo bus

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100

10 bits per Tx  
round up to unit

Working in a laboratory setting

	CANADA	U.S.	MEXICO	OTHER	TOTAL
1960-61	0.2	20	20	18	17
1961-62	0.5	3.5	2.5	2	1.5
1962-63	7	4	3	2	2

~~061925M1Z from Rk [w/2x exp 00:00-00:00]  
+38 b/min gram: Rx  
removed w/o 1st wash Rx~~

ಮೈಸೂರು ಮಹಾರಾಜರ ಕುರಿತು  
ಮೈಸೂರು ಮಹಾರಾಜರ ಕುರಿತು  
ಮೈಸೂರು ಮಹಾರಾಜರ ಕುರಿತು

行方(出)品名	4	2	2	1	1
アクリル系樹脂	5	3	1	2	1

4. Update these numbers to reflect the most current information available to effect of audit procedures

5

40769	604120	1231187	1662401	3407740A	2476148C
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## Abstract

Post Card  
number

Active Yr	10	8	10	12	7	13
Active Pts	43	+2	-4	94	14	13

State	Number of sealions per airport	Number of observations per unit
Alaska	1	1
California	1	1
Florida	1	1
Georgia	1	1
Hawaii	1	1
Idaho	1	1
Illinois	1	1
Indiana	1	1
Iowa	1	1
Kansas	1	1
Kentucky	1	1
Louisiana	1	1
Maine	1	1
Maryland	1	1
Massachusetts	1	1
Michigan	1	1
Minnesota	1	1
Mississippi	1	1
Missouri	1	1
Montana	1	1
Nebraska	1	1
Nevada	1	1
New Hampshire	1	1
New Jersey	1	1
New Mexico	1	1
New York	1	1
North Carolina	1	1
North Dakota	1	1
Ohio	1	1
Oklahoma	1	1
Oregon	1	1
Pennsylvania	1	1
Rhode Island	1	1
South Carolina	1	1
South Dakota	1	1
Tennessee	1	1
Texas	1	1
Utah	1	1
Vermont	1	1
Virginia	1	1
Washington	1	1
West Virginia	1	1
Wisconsin	1	1
Wyoming	1	1

101-110873

[illegible]

number of eligible technicians connections per supplier  
number of eligible technicians connections per supplier

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number of plus or minus cards

Aug 1-4

Excluded RV	8	15	25	12	21
excluded TX	20	24	24	24	22
excluded TX	12	10	24	24	21

These activities are essential for the health of the community. The results of the study are as follows:

2014年12月15日

Experiments	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
Experiments	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100

number of global knowledge connections per addressee

Step 1  
Step 2

[illegible]

number of gipsy blackpans constructed per seven gipsy-alor  
number of gipsy blackpans constructed per fabric  
number of gipsy new fabric